Pixie-16 MZ-TrigIO

Instruments That Advance The Art

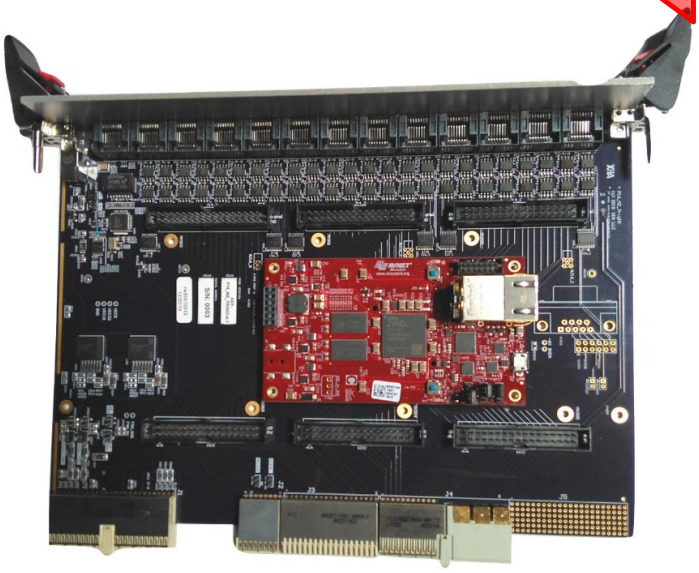
MZ-TrigIO

DRAFT

Clock and Trigger Distribution For Pixie-16 Systems

FEATURES

- **48 front panel LVDS input/output connections**
- **48+ Pixie-16 backplane trigger connections**
- **MicroZed Zynq processor with embedded Linux, acting as a standalone PC with built-in SD card drive, 1 GB RAM, USB host, Ethernet, webserver**
- **10/100M Ethernet, compatible with IEEE 1588 PTP and SyncE**
- **Sub-nanosecond Timing Resolution**
- **Desktop, rack mount, OEM**
- **Custom connections with I/O daughtercards**
- **Fully open source software and firmware with demo Vivado project**



OVERVIEW

The Pixie-16 MZ-TrigIO is a Zynq (FPGA+ARM) module combined with an input/output carrier board. The carrier board is primarily a 6U breakout board for the Pixie-16 custom PXI chassis backplane. It connects ~48 lines from the backplane to the Zynq FPGA. Another ~48 lines from the Zynq FPGA connect to front panel I/O via bidirectional LVDS buffers and RJ-45 connectors for CAT-5 cables. The backplane and front panel connections are also connected to 0.1” headers to allow direct access via cables or custom signal I/O via daughtercards.

The Zynq ARM Linux OS (Ubuntu 18) can be accessed via USB/UART on its native connectors but mainly via a PTP compatible 10/100M Ethernet port on the front panel. Simple Linux programs (C/C++) control the FPGA logic and make monitoring data available on a webpage hosted on the board. A PTP synchronized clock can become the Pixie-16 chassis master clock, and triggers can be issued at user specified date and time, synchronized over the network via PTP to tens of nanosecond precision.

Besides being operated in the Pixie-16 PXI chassis, the Pixie-16 MZ-TrigIO can also be operated as a standalone desktop unit.

APPLICATIONS

- **Trigger distribution for Pixie-16 systems**
- **Monitoring Pixie-16 operation via webserver**
- **General purpose coincidence and multiplicity logic (user programmable)**
- **LVDS-to-CMOS converter**
- **PTP controlled timing of trigger and control signals**

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