User's Manual

PXI Power Distribution Module

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X-Ray Instrumentation Associates

8450 Central Ave
Newark, CA 94560 USA

Phone: (510) 494-9020; Fax: (510) 494-9040
http://www.xia.com

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1 Overview

The PXI Preamplifier Power and Trigger Breakout Module (PXI PDM) is a module to support XIA's Pixie-4 data acquisition modules. It is manufactured in a 3U CompactPCI/PXI form factor and can reside in any peripheral slot (2-8) of a standard 3U chassis, together with Pixie-4 modules or by itself. Slot 2, the PXI Star Trigger slot, is the preferred location, as it allows the use of some additional functions.

Though manufactured in the CompactPCI/PXI form factor, the PXI PDM does not have a PCI interface and is thus not recognized by the PCI bus controller or host computer. It only uses power from the PCI backplane and connects to the PXI backplane lines used for clock and trigger distribution by Pixie-4 modules. The power is used to generate a low noise preamplifier power supply; the clock and trigger lines can be brought to the PXI PDM front panel to connect to external electronics.

The PXI PDM provides four principal functions, namely

- Preamplifier power supply for the detector
- Clock distribution
- Access to backplane trigger signals
- High Voltage suppy for the detector bias (optional)

2 Preamplifier Power Supply

The PXI PDM provides +/-12V and +/-24V power through a DB9 connector on its front panel. This enables a compact experimental setup of detector and Pixie-4 data acquisition boards without the need for external power supplies. Moreover, powering the detector and the Pixie-4 boards from the same source eliminates potential grounding problems.

The power supply output currents are rated according to the following table:

Supply Voltage	Maximum Current
+12V	100mA
-12V	100mA
+24V	40mA
-24V	40mA

Table 1: Maximum currents for the preamplifier power supply.

The pinout of the front panel DB9 connector follows the common pattern in nuclear instrumentation, shown in the table below. Some normally unused pins can carry logic signals from the backplane if the corresponding jumper is set.

Pin Number	Signal	Notes
1	GND	
2	GND	
3	EventTrigger	Only if Jumper 38 is set
4	+12V	
5	Veto	Only if Jumper 36 is set
6	-24V	
7	+24V	
8	Time	Only if Jumper 37 is set
9	-12V	

Table 2: Pinout of the DB9 front panel connector. See section 4 for a description of the signal lines

3 Clock Distribution

Note: This description assumes that the board has been modified after production. There should be an additional wire on the back side of the board near the clock jumpers.

In experimental setups with more than one Pixie-4 module, all Pixie-4 modules should run off the same clock to synchronize triggers and timestamps between them. There are a number of options to share clocks between Pixie-4 modules without the need for a PXI PDM module. The PXI PDM allows additional configurations. In particular, it allows the use of the low skew PXI clock from the PXI backplane, and it allows input from and output to external clock sources.

There are five possible clock sources for the PXI PDM:

1. The local clock crystal on the module
2. An external differential (LVDS) clock connected to the front panel
3. The PXI clock provided by the chassis. By default, it runs at a frequency of 10MHz and is only useful for Pixie-4 clock distribution if it has been overridden by a 37.5MHz clock signal.
4. A clock from a module distributed through a bussed backplane line
5. A clock from left neighboring module distributed through a daisy-chain

One of these clock sources can be selected for the PDM's local FPGA. A clock is required to distribute the trigger signals as described in section 4. The clock signal can also be distributed to other modules one of in four different ways:

1. The PDM always sends out a differential (LVDS) clock to the front panel
2. The PDM can override the PXI clock created by the backplane, which is distributed to all slots in the PXI chassis.
3. The PDM can send out the clock to a bussed backplane line to all slots in the chassis.
4. The PDM can send out the clock to the right neighboring slot .

	To local FPGA	**To front panel output**	**To PXI clock override**	**Output to right neighbor**	**To BUS clock output**
Local clock JP1: 3-1	always	always	JP5: 2-3	through FPGA	JP5: 2-1
Front panel input JP1: 4-6; JP6	always	always	JP5: 2-3	through FPGA	JP5: 2-1
PXI clock input JP1: 3-5	always	always	illegal jumper setting	through FPGA	JP5: 2-1
BUS input JP1: 4-2	always	always	JP5: 2-3	through FPGA	illegal jumper setting
Left neighbor input (if signal present)	not possible (use local)	not possible	not possible	with jumper bypass (disable FPGA output)	not possible

Table 3: Summary of clock distribution options for the PXI PDM. Choose one of the input options (rows) and one of the three backplane output options, as described in detail below.

The different options for clock distribution are summarized in Table 3 and explained in detail below. In practice, the following three options should cover most applications:

1. The PXI PDM is not used for clock distribution, and runs of its local clock, as described in section 3.1
2. The PXI PDM, with its local clock source, is used to override the PXI clock from the backplane to distribute the clock signal to all modules, as described in section 3.2.1
3. The PXI PDM is used to run all modules in the chassis from an external clock, as described in section 3.3.1

3.1 Local clock only

To run the PXI PDM from its local clock, independent of any other clocks in the system, set a shunt on jumper JP1 such that pins 1 and 3 are connected. Do not set jumpers JP3, JP4, and JP6 and do not set any shunt on jumper JP5. Any signal on the front panel clock input (pins 1 and 2 of the 2mm connector) will be ignored.

Note that the front panel clock output (pins 15 and 16 of the 2mm connector) always carries a differential clock signal (LVDS).
Furthermore, the daisy-chained clock output to the right neighbor (PXI_LBR0) is driven by the FPGA unless shunts on J10 are set correctly. To avoid driving conflicts, do not set Jumper JP10 (to connect left and right neighboring lines) if there is a signal source signal driving the clock line from the left, and remove jumper JP3 on the (right) neighboring Pixie-4 board.

3.2 PXI PDM is clock master

The PXI PDM can distribute its local clock to the other modules in the chassis in 3 different ways. An LVDS clock output signal is also available on pins 15 and 16 of the front panel I/O connector to distribute the clock to other chassis. Any signal on the front panel clock input (pins 1 and 2 of the 2mm connector) will be ignored. The three options for clock distribution are

3.2.1 Distribute local clock via PXI clock

If the PXI PDM resides in slot 2 of the chassis, it can override the 10MHz clock provided by the backplane with its local clock. The backplane will distribute the local clock with low skew buffering to each slot in the chassis. This is the preferred configuration if slot 2 is available.

To do so, set a shunt on jumper JP1 such that pins 1 and 3 are connected. Do not set jumpers JP3, JP4, and JP6. Set a shunt on jumper JP5 such that pins 2 and 3 (the middle and the upper pin) are connected.
To avoid conflicts with the daisy-chained backplane clock, either set the shunts on J10 to disable the clock output (see Table 4), or remove both Jumper JP10 on the PXI PDM and JP3 on the neighboring Pixie-4 module.

3.2.2 Distribute local clock via daisy-chained line

If slot 2 is not available, the daisy-chained clock output can be used to send the clock to the neighboring module, which will pass it on to its neighbor etc. For the PXI PDM to work as he clock master, all Pixie-4 modules have to be located to the right of the PXI PDM.

To do so, set a shunt on jumper JP1 such that pins 1 and 3 are connected. Do not set jumpers JP3, JP4, and JP6 and do not set any shunt on jumper JP5. Set the shunts on J10 to enable the clock output (see Table 4). Make sure the Pixie-4 boards are configured to use the daisy-chained clock as an input.

3.2.3 Distribute local clock via bussed line

If the PXI PDM can not sit in slot 2 or to the right of all Pixie-4 modules, it can send the external clock through a bussed clock line to all modules. This mode is not recommended for systems with more than three Pixie-4 modules.

To do so, set a shunt on jumper JP1 such that pins 1 and 3 are connected. Do not set jumpers JP3, JP4, and JP6. Set a shunt on jumper JP5 such that pins 1 and 2 (the lower and the middle pin) are connected
To avoid conflicts with the daisy-chained backplane clock, either set the shunts on J10 to disable the clock output (see Table 4), or remove both Jumper JP10 on the PXI PDM and JP3 on the neighboring Pixie-4 module.

3.3 External clock is clock master

The PXI PDM can use an external differential (LVDS) clock signal, connected to pins 1 and 2 of the front panel I/O connector for its local FPGA and distribute it to all modules in the chassis in 3 different ways. A repeated LVDS clock signal is available on pins 15 and 16 to distribute the clock to other chassis. The three options for clock distribution are

3.3.1 Distribute external clock via PXI clock

If the PXI PDM resides in slot 2 of the chassis, it can override the 10MHz clock provided by the backplane with the external clock. The backplane will distribute the external clock with low skew buffering to each slot in the chassis. This is the preferred configuration if slot 2 is available.

To do so, set a shunt on jumper JP1 such that pins 4 and 6 are connected. Set jumper JP6 but not jumpers JP3 and JP4. Set a shunt on jumper JP5 such that pins 2 and 3 (the middle and the upper pin) are connected.
To avoid conflicts with the daisy-chained backplane clock, either set the shunts on J10 to disable the clock output (see Table 4), or remove both Jumper JP10 on the PXI PDM and JP3 on the neighboring Pixie-4 module.

3.3.2 Distribute external clock via daisy-chained line

If slot 2 is not available, the daisy-chained clock output can be used to send the clock to the neighboring module, which will pass it on to its neighbor etc. For the PXI PDM to work as he clock master, all Pixie-4 modules have to be located to the right of the PXI PDM.

To do so, set a shunt on jumper JP1 such that pins 4 and 6 are connected. Set jumper JP6 but not jumpers JP3, JP4. Do not set any shunt on jumper JP5. Set the shunts on J10 to enable the clock output (see Table 4). Make sure the Pixie-4 boards are configured to use the daisy-chained clock as an input.

3.3.3 Distribute external clock via bussed line

If the PXI PDM can not sit in slot 2 or to the right of all Pixie-4 modules, it can send the external clock through a bussed clock line to all modules. This mode is not recommended for systems with more than two Pixie-4 modules.

To do so, set a shunt on jumper JP1 such that pins 4 and 6 are connected. Set jumper JP6 but not jumpers JP3, JP4. Set a shunt on jumper JP5 such that pins 1 and 2 (the lower and the middle pin) are connected.
To avoid conflicts with the daisy-chained backplane clock, either set the shunts on J10 to disable the clock output (see Table 4), or remove both Jumper JP10 on the PXI PDM and JP3 on the neighboring Pixie-4 module.

Note: Both the front panel clock input and the clock output are LVDS differential signals. The signal amplitude is about 400mV. The incoming clock is terminated with 100Ohm between the two differential lines if JP6 is set. The outgoing clock has to be terminated likewise at the receiving end.
For longer distances, a twisted or shielded cable is recommended, rather than the flat cable used for the trigger lines.

3.4 Clock master on backplane

In cases where another module in the chassis is the clock master, the PXI PDM can connect to that clock and bring it out to the front panel as a differential clock. Pins 15 and 16 of the I/O connector always carry the clock output signal. The clock for the local FPGA is always connected to the selected inputs. The backplane master clock input can be selected as follows:

3.4.1 PXI clock input

If the master clock is distributed through the PXI clock, set a shunt on jumper JP1 such that pins 3 and 5 are connected. Do not set jumpers JP3, JP4, and JP6. Do not set a shunt on jumper JP5. Any signal to the front panel clock input (pins 1 and 2 of the 2mm connector) will be ignored.

To avoid conflicts with the daisy-chained backplane clock, either set the shunts on J10 to disable the clock output (see Table 4), or remove both Jumper JP10 on the PXI PDM and JP3 on the neighboring Pixie-4 module.

3.4.2 Bussed clock input

If the master clock is distributed by another module through the bussed clock line, set a shunt on jumper JP1 such that pins 2 and 4 are connected. Do not set jumpers JP3, JP4, and JP6. Do not set a shunt on jumper JP5. Any signal to the front panel clock input (pins 1 and 2 of the 2mm connector) will be ignored.
To avoid conflicts with the daisy-chained backplane clock, either set the shunts on J10 to disable the clock output (see Table 4), or remove both Jumper JP10 on the PXI PDM and JP3 on the neighboring Pixie-4 module.

3.4.3 Daisy-chained clock input

In its current revision, the PXI PDM does not connect to daisy-chained clocks coming in from the left, neither for its local FPGA nor for distribution to other chassis.
It can be operated on its local clock and at the same time pass through the backplane clock signal from left to right if JP10 is set. However, if JP10 is set, the shunts on J10 should be set (see Table 4) to disable the FPGA from sending out its local clock to the right neighbor line, which would cause a conflict.

3.4.4 Other Clock Options

In principle, though rarely necessary, it is also possible to distribute the master clock back onto the backplane (e.g. the PXI PDM receives the master clock through the bussed clock line and sends it out through the PXI clock to other modules).
To do so, set the jumpers according to the clock input as described above. To send out the clock as a PXI clock, if the PXI PDM is in slot 2, set a shunt on jumper JP5 such that pins 2 and 3 (the middle and the lower pin) are connected. For a bussed clock, connect pins 1 and 2. To send out the clock to the right neighbor, set the shunts on J10 to enable the clock and remove JP10, but not JP3 on the neighboring Pixie-4 module.
Note that some jumper settings are illegal, as the same clock option can not be source and destination simultaneously.

4 Backplane Triggers

The trigger signals of the Pixie-4 modules on the backplane can be accessed through the I/O connector on the front panel of the PXI PDM. An FPGA between the backplane and the front panel connector acts as a configurable logic gate to implement combinations of backplane signals, which are then routed to the front panel.
For direct access to a few most common signals, three backplane lines are also included in the DB9 power connector, without going through the FPGA (see Table 2).

The configuration of the FPGA can be adapted to specific applications. Below we describe the standard configuration PDM 1.0, generated 6/11/2004. For custom configurations, contact XIA.

Note:
Care should be taken to only connect appropriate 3.3V signals at the front panel inputs and to avoid shorts on the signal outputs, as they are connected directly to the FPGA with no intermediate buffers!

The 30 pins of the front panel connector include input and output signals, ground and power, as listed in Table 5. The connector is a shrouded header with 2mm pitch. A matching receptacle is for example Molex part 87568-3091. Usually signals will be brought out to some external electronics with a 30x flat cable. The external electronics can then distribute clocks and triggers among all chassis.

With some limitations, inputs and outputs can also be daisy-chained with a 14x flat cable from chassis to chassis. For complete trigger distribution, the daisy-chain should be closed back from the last to the first chassis, however as described below, the Sync line can not be closed from the last to the first module. Furthermore, any external input signal (such as veto) has to be introduced at some point into the daisy-chain.

4.1 FPGA operation modes

In the standard FPGA configuration, the FPGA can be in different modes. The main difference between the modes is the disabling of certain backplane outputs, to avoid conflicts between the PXI PDM and another module on the backplane driving the same line. In addition, connections between the front panel and the backplane might differ if the PXI PDM is located in the most left, middle, or most right slot.
By setting shunts on the connector J10, these modes can be selected as described in Table 4.

Mode	Shunt connects	Function
“Pixie-4 ok”	Pins 8-9	Without shunt, all those backplane lines are disabled that are used for Pixie-4 functions that are not yet implemented. This is to avoid conflicts with accidentally driven lines. **Currently, these lines are always disabled**
“enable”	Pins 6-7	Without shunt, all backplane outputs are disabled. Backplane inputs are still active and are brought to the front panel
“left”	Pins 4-5	Set shunt to indicate that the PXI PDM is in the most left position in the chassis. Disables outputs to left neighbors and uses the alternative the Token Ring input on the backplane
“bypass”	Pins 2-3	Set shunt to indicate that the bypass shunts on jumpers JP10-22 are set to connect left and right neighboring lines, usually when module in middle position. Disables outputs on all neighboring lines (including clock).
“right”	Pins 0-1	Set shunt to indicate that the PXI PDM is in the most right position in the chassis. Disables outputs to right neighbors (including clock) and uses the alternative Token Ring output on the backplane

Table 4: Shunts on J10 to set FPGA modes. Shunts can be set simultaneously for all modes, except setting both “left” and “right”. Pin 0 of J10 is the upper right pin, closest to the backplane connector and to the edge of the board.
The clock output to the right neighbor is disabled if any of the following is true: a shunt is placed on pins 0-1, a shunt is placed on pins 2-3, or no shunt is placed on pins 6-7.

4.2 Description of Backplane Lines

The Pixie-4 trigger signals use several of the designated PXI lines on the backplane. These lines come in three different types: bussed lines, neighboring lines and the star trigger lines.

4.2.1 Bussed backplane lines

Bussed backplane lines connect all slots of a PXI backplane. (In a chassis with more than 8 slots, the bussed lines can be divided in several segments, see manufacturer’s details.) In the Pixie-4 trigger setup, four of these lines are used as wire-OR busses (active low with pullup) to distribute trigger and synchronization signals: FastTrigger, EventTrigger, Sync, and Time.

- FastTrigger signals that in at least one module an input signal pulse crossed over the trigger threshold. The FastTrigger signal is used to stop the FIFOs for waveform acquisition in all modules simultaneously.
- EventTrigger signals that the pulse passed pileup inspection and is indeed a pulse with a valid energy measurement. This signal causes an interrupt in the Pixie-4 DSP to read out and process the event data.
- Sync is used to start and stop runs synchronously. While a module is setting up a data acquisition run (clearing memory, resetting pointers, etc), it pulls this line low. When ready to take data, the line is released. The last module to release the line lets it go high, which signals a runstart to all modules. The first module to finish a run pulls the line low again to stop the data acquisition in all other modules.
- Time is currently unused

The PXI PDM connects the wire-OR bussed lines through its FPGA to an input and an output on the front panel. For all signals except Sync, the falling edge of an input pulse will create a ~100ns pulse on the corresponding backplane line. The front panel output is equal to the corresponding backplane line.
The Sync backplane line will be pulled low for as long as the front panel input is low. If the front panel input goes high, the backplane line may still be pulled low by a module in the chassis. The front panel output is equal to the backplane line.

Note: Since only one backplane line is used for run synchronization, it is not possible to inhibit runs externally (by pulling the backplane low through the PDM) and at the same time know if the Pixie-4 modules are not ready (pulling the line low themselves).
This means that in the current implementation, either the PDM output is used to know the status of the backplane, or the PDM input is used to inhibit data acquisition. Limited run synchronization in a multiple chassis system can be set up in 2 ways:

- Either the Sync inputs of all PDMs are controlled in parallel by external electronics, which inhibits data acquisition for an estimated time until all modules are assumed to be ready. While the run is in progress, the external electronics can monitor the signals from the Sync outputs, and stop the run whenever the first output goes low (by pulling the Sync inputs low).
- Alternatively, crates can be daisy-chained (Sync output of one PDM to Sync input of the following PDM). The daisy-chain can not be closed from the last to the first PDM as the system could be locked in an inhibited state. The modules and chassis have to be set up such that the first chassis is in control of the synchronization
  The Sync output of the PDM in first chassis is determined by state of the backplane line controlled by the Pixie-4 modules in the chassis. While the Pixie-4 moules are not ready to take data, the Sync output will be low and thus inhibit the second chassis, which in turn inhibits the following chassis and so on. When the Pixie-4 modules in the first chassis are ready, its backplane Sync line goes high and the modules in the first crate will begin taking data. The PDM Sync output line will also go high, and if all the Pixie-4 modules in the second chassis were ready before, data acquisition will begin in the second chassis at the same time, and also in any additional chassis further

down the daisy chain. When a module in the first chassis is finished with the run, it will inhibit all modules in its chassis and also further down the daisy-chain.

Full external run synchronization can be implemented by using 2 backplane lines in future software revisions.

The backplane lines for EventTrigger and Time are also directly accessible in the DB9 preamp power connector, if Jumpers JP37 and JP 38 are set. Jumper JP8 can be set to bypass the FPGA and bring the backplane FastTrigger line directly to the front panel I/O connector (pin 4).

Besides the above wire-OR lines, the Pixie-4 modules use two additional bussed backplane lines: Veto and TRreturn

- Veto has to be driven by an external source. If high, it inhibits event triggers of Pixie-4 modules that have the GFLT bit set. There is no pullup on this line.
  The PXI PDM connects a front panel input through its FPGA to the backplane veto line. Jumper JP32 should be set to connect the front panel input directly to the front panel output for distribution to other chassis. The backplane signal Veto is also directly accessible in the DB9 preamp power connector, if Jumper JP36 is set.

- TRreturn is currently unused, output disabled. It is reserved to implement a token ring for multiplicity information.

The FPGA also connects to all other bussed lines on the backplane, which are unused in the current Pixie-4 configuration (outputs disabled). These signals are currently not available on the front panel.

4.2.2 Neighboring backplane lines

Neighboring or daisy-chained backplane lines connect a module to its left and right neighbors. (In slot 2, which has no left neighbor, the lines going to the left are used for the Star Trigger.)

4.2.2.1 Clock

One pair of these neighboring lines (PXI_LBR0 and PXI_LBL0) is used for clock distribution. On a Pixie-4 module, the clock coming in from the left neighbor can be configured as the module’s clock input. The module’s clock is always sent out to the right neighbor, independent of the clock source.

In the PXI PDM, the incoming clock from the left neighbor is not used. The PDM's FPGA will send out its clock to the right neighbor, unless it is disabled by setting a shunt on J10 in any of the following ways: connecting pins 0-1 ("right" mode), connecting pins 2-3 ("bypass" mode), or disconnecting pins 6-7 (not "enabled" mode).

To pass through the clock from a left neighbor to a right neighbor, set a shunt on JP10 to directly connect left input to right output, and connect pins 2-3 on J10 to put the FPGA in "bypass" mode (which disables driving the output).

4.2.2.2 Trigger

In the Pixie-4 trigger setup, three of the neighboring lines are reserved to distribute trigger information: Token Ring and Nearest Neighbor (2 lines). They are not yet implemented in the current Pixie software release. In the PXI PDM, the outputs to these backplane lines are currently disabled.

4.2.2.3 Other lines

The FPGA also connects to all other PXI neighbor lines on the backplane, which are unused in the current Pixie-4 configuration (outputs disabled). These signals are currently not available on the front panel.
For all PXI neighbor lines, there are bypass jumpers (JP10-22) on the PXI PDM, to directly connect lines to/from the left to the corresponding lines from/to the right. If these jumpers are used, the connect pins 2-3 on J10 to put the FPGA in "bypass" mode (which disables driving the outputs).

4.2.3 Star Trigger lines

Designated "Star Trigger" lines on the PXI backplane connect each module to slot 2. These lines can be used by the Pixie-4 modules to share trigger or multiplicity information (not yet implemented). If the PDM sits in slot 2, it can access these lines, and bring out an AND of the signal from all modules to the front panel. Set the shunts on J10 to indicate the module is in the "left" position.

5 Application Example

As an example, we consider the case of two chassis with one Pixie-4 and one PXI PDM each. Both chassis will also have their own system controller to set up and control the Pixie-4 modules.

In this setup, chassis 1 will be the Sync master and the PDM in chassis 1 will be the clock master. Triggers are distributed from all modules to all modules. The Veto signal is driven by an external source. In each chassis, the system controller sits in slot 1, the PDM in slot 2, and the Pixie-4 module in slot 3.

Both Pixie-4 modules in chassis 1 and chassis 2 are configured to receive their clock input from the left neighbor (the PDM) by setting a shunt on Jumper JP3 and no shunts on JP1 or JP2.

On PDM 1, in chassis 1, the clock master, we use the local clock crystal as the clock source, which is connected to the front panel clock output and the local FPGA. Thus we set a shunt on JP1 to connect pins 1 and 3 and no shunts on JP 3,4,5, or 6. To enable the clock output from the FPGA to the right neighbor, we set a shunt on J10 such that pins 6 and 7 are connected ("enable" mode[1]). A shunt is placed on JP 32 to pass through the Veto signal from front panel input to output. All other jumpers (JP8, JP10-22, JP 30-31, JP33-34, JP35-38) have no shunts.

On PDM 2, in chassis 2 we use the front panel clock input as the clock source, which is connected to the local FPGA. (The front panel output is also connected, but is ignored as an input in PDM 1.) Thus we set a shunt on JP1 to connect pins 4 and 6, a shunt on JP6 to terminate the incoming LVDS clock, and no shunts on JP 3,4, or 5. To enable the clock output from the FPGA to the right neighbor, we set a shunt on J10 such that pins 6 and 7 are connected ("enable" mode). A shunt is placed on JP 32 to pass through the Veto signal from front panel input to output. All other jumpers (JP8, JP10-22, JP 30-31, JP33-34, JP35-38) have no shunts.

The PDM front panel connectors are connected input to output with a flat cable (1mm pitch). For each PDM module, there is a 30x 2mm connector, in which the first 14 lines are the inputs, the second 14 lines are the outputs, and the last 2 lines are power, not used for signal distribution. A cable can be fabricated with pieces of 14x flat cable: one strand of flat cable goes from the outputs of the first connector to the inputs of the second; a second strand from the outputs of the second to the inputs of the first. In the second strand, the Sync output line (of PDM 2) is cut. Furthermore, to introduce a veto signal from an external source, the veto line is cut in an arbitrary position and one of the ends connected to the external source. (Alternatively, JP36 could be set and the external signal introduced in pin 5 of the DB9 connector in both PDMs)

The Pixie-4 modules can be set up as usual through the user software. One or both can be enabled for triggers, and to share triggers through backplane and PDM they should "respond to group trigger".
When starting data acquisition runs, the checkbox "start/stop modules simultaneously" should be checked. Since chassis 1 is the Sync master, runs must be started in chassis 2 first, which will be kept waiting by chassis 1 until a run is started in chassis 1.

During the run, while the veto line is high, no events are recorded in either of the modules.

[1] Pins 4-5 can be connected in addition to put the module in "left"mode, but this is only important if some of the not yet implemented functions were to be used.

If the run is finished in chassis 1, it will also stop the run in chassis 2 through the Sync line, but not the other way round. Therefore the system should be set up such that the module in chassis 1 will always finish the run first, i.e. it receives much more pulses than the module in chassis 2.

6 Optional High Voltage

The PXI PDM has a double slot High Voltage variant providing a maximum of 0.8mA of current for voltages up to 1.2kV. This variant comes with factory set positive or negative polarity.

6.1 Operation

High voltage bias for the detector is provided at the SHV connector labeled “”HIGH VOLTAGE OUT”. For detectors with thermal shutdown protection, connect the shutdown line to the LEMO connector labeled “L/N INHIBIT”. Make sure the jumper settings for the shutdown logic matches your particular detector. When the PXI PDM is switched on, either the “+” or the “-“ LED on the front panel is green, indicating the module polarity. The HV bias can be adjusted from 0 to 1.2kV on the front panel. Use a small screwdriver to turn the potentiometer labeled “ADJUST” to set the voltage. The absolute set voltage is shown in the LCD display. To turn on the high voltage, push the red “ENABLE” button. The LCD display will now show the actual absolute output voltage, ramping up from zero to the set voltage, and the “ENABLED” LED will turn red. Pushing the button a second time will ramp down the high voltage back to zero. Due to detector sensitivity, please refer to your detector user’s manual for bias voltage ramp steepness before making any connection.

6.2 HV shutdown (JP35).

Detectors with thermal shutdown protection usually come in two variants: Either logic high (one) indicates shutdown or logic low (zero) indicates shutdown. In order to match the shutdown circuitry to either variant, set JP35 to the logic level indicating the shutdown.

7 Default Jumper settings

By default, jumpers should be set as follows:

Jumper	Setting	Function	Caution
JP1	connect pins 1-3	local clock source	
JP3, JP4	remove	never used	
JP5	remove	no clock to backplane	
JP6	set	incoming LVDS clock termination	
JP8	remove	no FPGA bypass for Fast Trigger to front	
JP10-22	remove	bypass daisy-chained lines left to right	If set, disable FPGA outputs by setting shunts on J10 to “bypass” mode
JP30-31	remove	FPGA bypass for front panel input to output	Do not set. Will cause driver conflict between FPGA and input
JP32	set	FPGA bypass for front panel input to output for Veto signal	
JP33-34	remove	FPGA bypass for front panel input to output	Do not set. Will cause driver conflict between FPGA and input
JP35	remove	HV inhibit polarity - optional	
JP36-38	remove	connect backplane trigger to unused DB9 lines	Do not set if detector uses DB9 lines; do not use as input if FPGA “enabled” to drive backplane
J10	do not connect pins 8-9	reserved to disable output on reseverd lines	<currently unused>
	connect pins 6-7	if connected, globally enables FPGA outputs to backplane	do not use DB9 as inputs to backplane when FPGA outputs are enabled (remove JP36-38)
	do not connect pins 2-3	if connected, disables FPGA output on daisy-chained lines	must be connected when any of JP10-22 are used to bypass daisy-chained lines
	do not connect pins 0-1, 4-5	routes and disables lines according to module position	

8 Front Panel Connector Pinout

Front panel pin	Split cable line	Front panel connection type	Backplane pin name	Backplane connection type	Pixie function
1	1A	Clock In	LBR0, TRIG7, or PXI CLK	to right, bussed, or all	clock (depening on jumper setting
2	2A	Clock In*			
3	3A	GND			
4	4A	Input	TRIG0	bussed	Fast Trigger
5	5A	Input	TRIG1	bussed	Event Trigger
6	6A	Input	TRIG2	bussed	Veto
7	7A	Input	TRIG3	bussed	Sync
8	8A	Input	TRIG4	bussed	Time
9	9A	Input	LBR8 or TRIG5[1]	to right (or most left)	Token Ring
10	10A	GND			
11	11A	Input	LBR10[2]	to right	Nearest neighbor 1
12	12A	Input	LBL9[2]	to left	Nearest neighbor 0
13	13A	reserved			
14	14A	reserved			
15	1B	Clock Out			
16	2B	Clock Out*			
17	3B	GND			
18	4B	Output	TRIG0	bussed	Fast Trigger
19	5B	Output	TRIG1	bussed	Event Trigger
20	6B	Output	N/A[3]		Veto
21	7B	Output	TRIG3	bussed	Sync
22	8B	Output	TRIG4	bussed	Time
23	9B	Output	LBL8 or TRIG5[1]	from left (or most right)	Token Ring
24	10B	GND			
25	11B	Output	LBR9[2]	from right	Nearest neighbor 0
26	12B	Output	LBL10[2]	from left	Nearest neighbor 1
27	13B	Output	LBL0..5	from slot 3..8	AND of Star Triggers
28	14B	reserved			<test pulse out>
29	N/A	3.3V			
30	N/A	5V			

Table 5: Pinout of the 2mm front panel I/O connector. The signals can either be brought out to external electronics, or inputs and outputs can be connected from PDM to PDM with a split cable.
Notes: 1) For Token Ring, set jumpers according to module position. Currently not implemented
2) The NN distribution only works fully only for 2 chassis. Currently not implemented.
3) Veto out should connect directly to Veto in via JP32; not driven by FPGA or backplane
When looking at the front panel, pin 1 is to the top and right.